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☐ 1. Document ID: US 20040010464 A1

Using default format because multiple data bases are involved.

L2: Entry 1 of 24 File: PGPB Jan 15, 2004

PGPUB-DOCUMENT-NUMBER: 20040010464
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040010464 A1

TITLE: Communication device and method for implementing communication on a wide area network

PUBLICATION-DATE: January 15, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Boaz, John	McKinney	TX	US	

US-CL-CURRENT: 705/40

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030183934 A1

L2: Entry 2 of 24 File: PGPB Oct 2, 2003

DOCUMENT-IDENTIFIER: US 20030183934 A1
TITLE: Method and apparatus for stacking multiple die in a flip chip semiconductor package

Detail Description Paragraph:
[0025] Although the example embodiment of FIG. 5 includes a graphics accelerator and a system logic device sharing a package in accordance with the example embodiment described in connection with FIG. 3, other embodiments are possible with any of a wide range of devices being combined. For example, a die including a cache memory may be coupled with a die including a system logic (chipset) device having a cache controller. Another example may include a die including a graphics memory coupled with a die including a graphics controller.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20020093507 A1

L2: Entry 3 of 24 File: PGPB Jul 18, 2002

DOCUMENT-IDENTIFIER: US 20020093507 A1
TITLE: Multi-mode graphics address remapping table for an accelerated graphics port device

Detail Description Paragraph:
[0159] AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20010049771 A1

L2: Entry 4 of 24 File: PGPB Dec 6, 2001

DOCUMENT-IDENTIFIER: US 20010049771 A1
TITLE: DYNAMIC REPLACEMENT TECHNIQUE IN A SHARED CACHE

Detail Description Paragraph:
[0036] Referring to FIG. 3, an illustrative but not limiting block diagram of a multimedia processor system is depicted practiced in accordance with the principles of the present invention. A highly integrated multimedia processor 134, preferably formed on a unitary silicon die, includes a central processing unit (CPU) 136 having integer and floating point units and register files in accordance with the x86 architecture, a graphics unit 138, a shared L2 cache 140, a four port bus interface unit 142, a memory controller 144 and a I/O interface unit 146. The bus interface unit 142 couples together the CPU 136, the graphics unit 138, the L2 cache 140, the memory controller 144 and the I/O interface unit 146. The CPU 136 shares a single bus with the L2 cache 140 to the bus interface unit (BIU) 142. FIG. 3 logically depicts requests from the CPU 136 over the shared bus to the BIU 142 as passing through the shared L2 cache 140. The I/O interface unit 146 provides a fast interface between the processor 134 and a chipset bridge 147.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 20010012015 A1

L2: Entry 5 of 24 File: PGPB Aug 9, 2001

DOCUMENT-IDENTIFIER: US 20010012015 A1

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TITLE: Multi-function controller and method for a computer graphics display system

Detail Description Paragraph:
[0025] Referring to FIG. 3, the multi-function controller 111 is shown in detail and comprises a combined PCI bridge and cache controller 114, a communications link 126, and a unified graphics/video controller 120. The multi-function controller 111 can be a single chip or several chips, and, in one embodiment, all the components of the combined PCI bridge/cache controller are integrated into one chip and all the components of the unified graphics/video controller are integrated into another chip.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 6. Document ID: US 6591347 B2

L2: Entry 6 of 24 File: USPT Jul 8, 2003

DOCUMENT-IDENTIFIER: US 6591347 B2
TITLE: Dynamic replacement technique in a shared cache

Detailed Description Text (7):
Referring to FIG. 3, an illustrative but not limiting block diagram of a multimedia processor system is depicted practiced in accordance with the principles of the present invention. A highly integrated multimedia processor 134, preferably formed on a unitary silicon die, includes a central processing unit (CPU) 136 having integer and floating point units and register files in accordance with the x86 architecture, a graphics unit 138, a shared L2 cache 140, a four port bus interface unit 142, a memory controller 144 and a I/O interface unit 146. The bus interface unit 142 couples together the CPU 136, the graphics unit 138, the L2 cache 140, the memory controller 144 and the I/O interface unit 146. The CPU 136 shares a single bus with the L2 cache 140 to the bus interface unit (BIU) 142. FIG. 3 logically depicts requests from the CPU 136 over the shared bus to the BIU 142 as passing through the shared L2 cache 140. The I/O interface unit 146 provides a fast interface between the processor 134 and a chipset bridge 147.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 7. Document ID: US 6513099 B1

L2: Entry 7 of 24 File: USPT Jan 28, 2003

DOCUMENT-IDENTIFIER: US 6513099 B1
TITLE: Enhanced graphics cache memory

Detailed Description Text (6):
Memory bridge 302 includes a cache memory 314 and a cache controller 316. Cache memory 314 and cache Controller 316 are preferably included as part of the same chip or chipset that implements memory bridge 302. Cache controller 316 accepts

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memory requests from processor cache combination 304, PCI bus 308 and graphics processor 310. Cache controller 316 translates these requests into appropriate interactions with system memory 306.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 8. Document ID: US 6483516 B1

L2: Entry 8 of 24 File: USPT Nov 19, 2002

DOCUMENT-IDENTIFIER: US 6483516 B1
TITLE: Hierarchical texture cache

Detailed Description Text (7):
Referring to FIG. 3, an illustrative but not limiting block diagram of a multimedia processor system is depicted practiced in accordance with the principles of the present invention. A highly integrated multimedia processor 134, preferably formed on a unitary silicon die, includes a central processing unit (CPU) 136 having integer and floating point units and register files in accordance with the x86 architecture, a graphics unit 138, a shared L2 cache 140, a four port bus interface unit 142, a memory controller 144 and a I/O interface unit 146. The bus interface unit 142 couples together the CPU 136, the graphics unit 138, the L2 cache 140, the memory controller 144 and the I/O interface unit 146. The CPU 136 shares a single bus with the L2 cache 140 to the bus interface unit (BIU) 142. FIG. 3 logically depicts requests from the CPU 136 over the shared bus to the BIU 142 as passing through the shared L2 cache 140. The I/O interface unit 146 provides a fast interface between the processor 134 and a chipset bridge 147.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 9. Document ID: US 6480198 B2

L2: Entry 9 of 24 File: USPT Nov 12, 2002

DOCUMENT-IDENTIFIER: US 6480198 B2
TITLE: Multi-function controller and method for a computer graphics display system

Detailed Description Text (7):
Referring to FIG. 3, the multi-function controller 111 is shown in detail and comprises a combined PCI bridge and cache controller 114, a communications link 126, and a unified graphics/video controller 120. The multi-function controller 111 can be a single chip or several chips, and, in one embodiment, all the components of the combined PCI bridge/cache controller are integrated into one chip and all the components of the unified graphics/video controller are integrated into another chip.

CLAIMS:

4. The controller of claim 1 wherein the unified graphics controller is integrated

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into a single chip and the bus bridge and the cache controller form a combined bus bridge/cache controller integrated into a single chip.

5. The controller of claim 4 wherein the unified graphics controller and the combined bus bridge/cache controller form a multi-function controller integrated into a single chip.

10. Document ID: US 6247107 B1

L2: Entry 10 of 24 File: USPT Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6247107 B1
TITLE: Chipset configured to perform data-directed prefetching

Detailed Description Text (8):
Chipset 12 provides an interface between microprocessor 10, main memory 14, graphics controller 18, L2 cache 38, and devices attached to PCI bus 24. When an operation is received from one of the devices connected to chipset 12, chipset 12 identifies the target of the operation (e.g. a particular device or, in the case of PCI bus 24, that the target is on PCI bus 24). Chipset 12 routes the operation to the targeted device. In the case of a memory access, chipset 12 checks for a hit in L2 cache 38 prior to or in parallel with accessing main memory 14 via memory bus 16. L2 cache 38 provides lower latency access to data/instructions stored therein as compared to main memory 14. Typically, as data/instruction bytes are transferred to microprocessor 10, the data is also stored in L2 cache 38 on the assumption that the data may be accessed again. L2 cache 38 is referred to as "L2" because microprocessor 10 may also employ an internal cache. Chipset 12 generally translates an operation from the protocol used by the source device or bus to the protocol used by the target device or bus.

11. Document ID: US 6052133 A

L2: Entry 11 of 24 File: USPT Apr 18, 2000

DOCUMENT-IDENTIFIER: US 6052133 A
TITLE: Multi-function controller and method for a computer graphics display system

Detailed Description Text (7):
Referring to FIG. 3, the multi-function controller 111 is shown in detail and comprises a combined PCI bridge and cache controller 114, a communications link 126, and a unified graphics/video controller 120. The multi-function controller 111 can be a single chip or several chips, and, in one embodiment, all the components of the combined PCI bridge/cache controller are integrated into one chip and all

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the components of the unified graphics/video controller are integrated into another chip.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 12. Document ID: US 5999743 A

L2: Entry 12 of 24 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5999743 A
TITLE: System and method for dynamically allocating accelerated graphics port memory space

Detailed Description Text (107):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 13. Document ID: US 5999198 A

L2: Entry 13 of 24 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5999198 A
TITLE: Graphics address remapping table entry feature flags for customizing the operation of memory pages associated with an accelerated graphics port device

Detailed Description Text (94):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 14. Document ID: US 5990914 A

L2: Entry 14 of 24 File: USPT Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5990914 A
TITLE: Generating an error signal when accessing an invalid memory page

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Detailed Description Text (109):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

☐ 15. Document ID: US 5959689 A

L2: Entry 15 of 24 File: USPT Sep 28, 1999

DOCUMENT-IDENTIFIER: US 5959689 A
TITLE: Multi-media processor architecture with high performance-density

Brief Summary Text (5):
Texas Instruments has recently introduced a fully programmable digital signal processor, called the Multimedia Video Processor (MVP) TMS320C80. The MVP accommodates on a single semiconductor substrate one 100 MFLOP (million of floating-point operations per second) floating-point fully programmable RISC processor, four uniform, fully programmable 500 MOPS (million of operations per second) parallel processors (DSPs) with multiple data streams connected via a cross-bar network to 25 banks of 2K Byte SRAM for data and instruction caches, and an I/O controller for 400M Byte/sec off-chip communication. The RISC processor handles system control and communication with external processors. Since it is the only one with a floating-point unit, the RISC processor also is the preferred processor for performing floating-point-intensive computations. The DSPs are fully programmable in C or in assembly, and are especially suited for execution of multiply-accumulate-intensive algorithms. Each of the DSPs can execute 3 to 15 RISC instructions in parallel each cycle. The full programmability, similar to that of today's general-purpose processors, supports the dynamic selection among a variety of image compression techniques such as JPEG and MPEG. The full programmability is to allow the processors to perform virtually any task. See, for example, "The MVP: A Single-Chip Multiprocessor for Image and Video Applications", R. J. Gove, SID 94 Digest pp. 637-640, "A Single-Chip Multiprocessor For Multimedia: The MVP", K. Guttag et al., IEEE Computer Graphics & Applications, November 1992, pp. 53-64, or "A Single Chip Multimedia Video Processor", K. Balmer et al., Proc. of the IEEE 1994 Custom Integrated Circuits Conference, San Diego, Calif., May 1-4, 1994, pp. 91-94.

☐ 16. Document ID: US 5953746 A

L2: Entry 16 of 24 File: USPT Sep 14, 1999

DOCUMENT-IDENTIFIER: US 5953746 A

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**** See image for Certificate of Correction ****
TITLE: Method and apparatus for dynamically resizing a frame buffer in a shared memory buffer architecture system

Detailed Description Text (6):
FIG. 3 shows one exemplary embodiment of the chipset 10 for use in the invention. It will be recognized by one of ordinary skill in the art that the individual components of chipset 10 could be constituted discretely. In this exemplary embodiment, these components are, however, grouped as a unit. Arbitration unit 21 receives addresses from the CPU bus 2 and arbitrates whether the address should be sent to memory and cache controller 20 or to the bridge 25 to be forwarded to the I/O bus 8. The memory and cache controller 20 provides an interface between the CPU 1 and the physical memory 4. Memory arbiter 26 arbitrates between the memory controller 20 and the graphics controller 15 for access to the memory bus 9. Memory arbiter 26 can be discrete or combined with arbitration unit 21. In an alternative embodiment, memory arbiter may be omitted entirely and the graphics controller 15 may forward its frame buffer accesses back through bridge 25 to be handled by memory controller 20.

17. Document ID: US 5936640 A

L2: Entry 17 of 24 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5936640 A
TITLE: Accelerated graphics port memory mapped status and control registers

Detailed Description Text (110):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

18. Document ID: US 5933158 A

L2: Entry 18 of 24 File: USPT Aug 3, 1999

DOCUMENT-IDENTIFIER: US 5933158 A
TITLE: Use of a link bit to fetch entries of a graphic address remapping table

Detailed Description Text (101):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset

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perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 19. Document ID: US 5915265 A

L2: Entry 19 of 24 File: USPT Jun 22, 1999

DOCUMENT-IDENTIFIER: US 5915265 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for dynamically allocating and resizing the dedicated memory in a shared memory buffer architecture system

Detailed Description Text (6):
FIG. 3 shows one exemplary embodiment of the chipset 10 for use in the invention. It will be recognized by one of ordinary skill in the art that the individual components of chipset 10 could be constituted discretely. In this exemplary embodiment, these components are, however, grouped as a unit. Arbitration unit 21 receives addresses from the CPU bus 2 and arbitrates whether the address should be sent to memory and cache controller 20 or to the bridge 25 to be forwarded to the I/O bus 8. The memory and cache controller 20 provides an interface between the CPU 1 and the physical memory 4. Memory arbiter 26 arbitrates between the memory controller 20 and the graphics controller 15 for access to the memory bus 9. Memory arbiter 26 can be discrete or combined with arbitration unit 21. In an alternative embodiment, memory arbiter may be omitted entirely and the graphics controller 15 may forward its frame buffer accesses back through bridge 25 to be handled by memory controller 20.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 20. Document ID: US 5914730 A

L2: Entry 20 of 24 File: USPT Jun 22, 1999

DOCUMENT-IDENTIFIER: US 5914730 A
TITLE: System and method for invalidating and updating individual GART table entries for accelerated graphics port transaction requests

Detailed Description Text (101):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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21. Document ID: US 5914727 A

L2: Entry 21 of 24 File: USPT Jun 22, 1999

DOCUMENT-IDENTIFIER: US 5914727 A
TITLE: Valid flag for disabling allocation of accelerated graphics port memory space

Detailed Description Text (100):
AGP requests may range in size from 8 bytes to 32 quad words (QW) for reads and up to 8 QW for writes. This means it is impossible for the graphics controller to issue all requests on cache line boundaries. It is preferred that the chipset perform combined reordering of reads to minimize the performance impact of requests less than 4 QW in size.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

22. Document ID: US 5790849 A

L2: Entry 22 of 24 File: USPT Aug 4, 1998

DOCUMENT-IDENTIFIER: US 5790849 A
TITLE: Method and apparatus to permit the boot of a shared memory buffer architecture employing an arbitrary operating system

Detailed Description Text (6):
FIG. 3 shows one exemplary embodiment of the chipset 10 for use in the invention. It will be recognized by one of ordinary skill in the art that the individual components of chipset 10 could be constituted discretely. In this exemplary embodiment, these components are, however, grouped as a unit. Arbitration unit 21 receives addresses from the CPU bus 2 and arbitrates whether the address should be sent to memory and cache controller 20 or to the bridge 25 to be forwarded to the I/O bus 8. The memory and cache controller 20 provides an interface between the CPU 1 and the physical memory 4. Memory arbiter 26 arbitrates between the memory controller 20 and the graphics controller 15 for access to the memory bus 9. Memory arbiter 26 can be discrete or combined with arbitration unit 21. In an alternative embodiment, memory arbiter may be omitted entirely and the graphics controller 15 may forward its frame buffer accesses back through bridge 25 to be handled by memory controller 20.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

23. Document ID: US 5572655 A

L2: Entry 23 of 24 File: USPT Nov 5, 1996

DOCUMENT-IDENTIFIER: US 5572655 A

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TITLE: High-performance integrated bit-mapped graphics controller

Detailed Description Text (6):
FIG. 2 is a block diagram of a single-chip bit-mapped graphics display controller 200 according to the present invention. A video controller core 206, cache memory 207a, memory access control functional block 207b, a video shift register 208, and a 1 Megabyte DRAM video frame buffer memory 230 are integrated together on one chip. The boundaries of the chip 200 are indicated by a dashed line. The video controller core 206 provides basic video signal timing and interfaces to a host processor (computer) via control lines 215, address lines 220 and data lines 225. A master timing signal 210 (essentially a master clock signal) provides a frequency reference to the video controller core 206 for the generation of basic video timing and synchronization signals 246. The video controller core 206 accesses pixel data in the video frame buffer memory 230 via the cache memory 207a. The video controller core 206 accesses video frame buffer memory 230 (as commanded by the host computer) via the cache memory 207a across lines 262. The cache memory 207a is optional, but provides improved access to the video frame buffer memory 230 over comparable FIFO memory interfaces (such as that depicted in FIG. 1). The cache memory is based upon a (relatively) small high-speed (e.g., 10-20 ns) static RAM buffer. Any of a variety of suitable cache memory techniques, (e.g., direct-mapped, set-associative, etc.) may be used. Cache memories are widely known in the art, and will not be further elaborated upon herein.

☐ 24. Document ID: NN9301257

L2: Entry 24 of 24 File: TDBD Jan 1, 1993

TDB-ACC-NO: NN9301257

DISCLOSURE TITLE: Instruction Set for RCS Microsequencer.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, January 1993, US

VOLUME NUMBER: 36
ISSUE NUMBER: 1
PAGE NUMBER: 257 - 259

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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